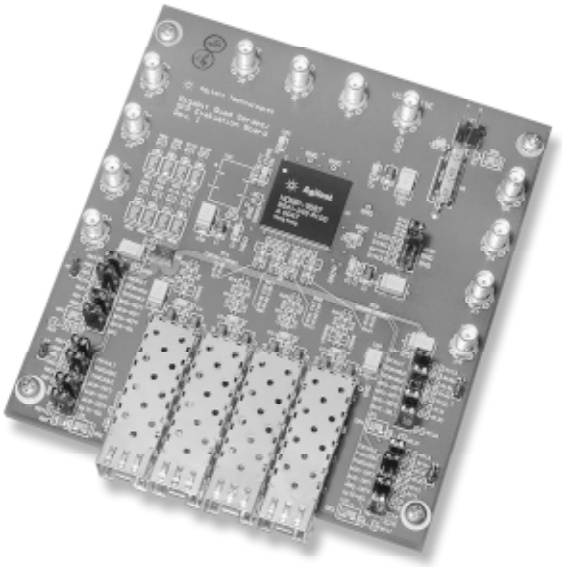
Application Note For GigaBit Ethernet Physical Layer Solution Utilizing Small Form Factor Pluggable (SFP) Optical Transceivers and Quad-Channel SerDes

Application Note 1243

Introduction

Agilent Technologies' objective in creating this application note is to generate a ready-to-use physical layer solution and experience-based design guidelines that enable our customers to successfully design Agilent components into their 1.25 GBd GigaBit Ethernet applications. In this case, Agilent introduces the Small Form-Factor Pluggable (SFP) optical transceivers (HFBR-5701L/5710L) and Quad-Channel SerDes (HDMP-1687), which are demonstrated in a reference design for this purpose as documented in reference design application note 1242.



Contents

Section 1. A Brief Introduction to GigaBit Ethernet

Section 2. Introduction to HFBR-5701L/5710L and HDMP-1687
- 2.1. HFBR-5701L/5710L
- 2.2. HDMP-1687

Section 3. Detailed Description of the 1.25 GBd Reference Design Considerations
- 3.1. Reference Design Guidelines and Printed Circuit Board (PCB) Layout Description
- 3.2. High Speed Input/Output (I/O) Transmission Line Details
- 3.3. Interpreting Jitter (Rj, Dj, and Tj)
- 3.4. Multi-Rate Compatibility (1.25 GBd and 1.0625 GBd)
- 3.5. Electromagnetic Interference (EMI)
- 3.6. Thermal Design Considerations
- 3.7. Power Supply Noise Rejection

Section 4. Reference Design Testing at 1.25 GBd

Section 5. Conclusions and Recommendations

Section 6. References

Appendices

A. Test Configuration

Section 1.

A Brief Introduction to GigaBit Ethernet

GigaBit Ethernet (GBE) is a high speed, network and physical layer specification for Local Area Network (LAN) applications. It is defined in the IEEE 802.3 2000 Edition specification per Reference 1. A typical LAN may include Switch to Switch Interfaces, Switched Backplane Applications, and File Server Interfaces. LAN applications with multi-rate switching from 10BASE-X, to 100BASE-X, to 1000BASE-SX (i.e., GBE) are described in the training materials found in Reference 2.

The physical layer is typically made up of a Media Access Control (MAC) IC, a Serializer-Deserializer (SerDes), and an Optical Transceiver as shown in Figure 1. Agilent Technologies is currently producing HDMP-1687 which is a Quad Channel SerDes and HFBR-5701L/5710L which is the latest Optical Transceiver for GBE applications.

Section 2.
Introduction to HFBR-5701L/5710L and HDMP-1687

2.1. HFBR-5701L/5710L

Description
The HFBR-5701L is compliant with both GBE (IEEE 802.3) and Fibre Channel (100-M5-SN-I and 100-M6-SN-I), Reference 1, 3, whereas the HFBR-5710L is compliant with only GBE (IEEE 802.3). Both transceivers are compliant with the Small Form Pluggable (SFP) Multiple Source Agreement (MSA). SFP transceivers can be inserted or removed from a host chassis without removing power from the host system (i.e., controlled hot plugging). Further, the LC fiber connectors enable the reduced size of the SFP. For a more detailed description regarding the HFBR-5701L/5710L, please visit the Agilent WebSite and look for the Product, Reliability, and Characterization Data Sheets which can be found in Reference 4.

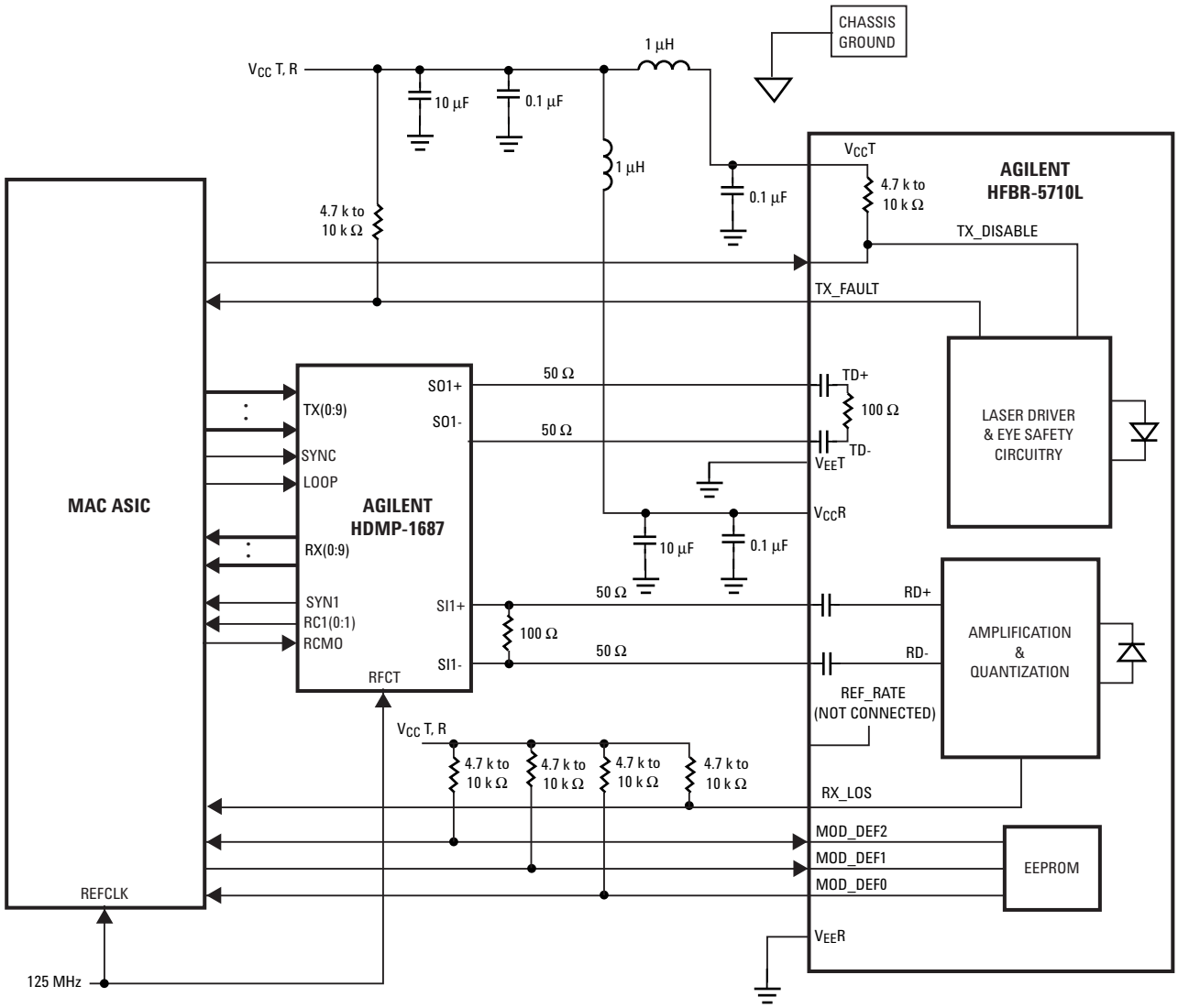


Figure 1. Typical GigaBit Ethernet Physical Layer Implementation Including Network Layer (MAC) IC

Transmitter Section
The transmitter section consists of an 850 nm VCSEL in an optical subassembly (OSA), which mates to the fiber cable via standard LC ports. The VCSEL OSA is driven by a silicon IC, which converts differential logic, signals into an analog laser diode drive current. This Tx driver circuit regulates the average optical power. The regulated light output will maintain a nearly constant optical power with a 8B10B encoded data pattern.

Receiver Section
The receiver includes a PIN photo-diode mounted together with a trans-impedance preamplifier IC in an OSA. This OSA is mated to a custom IC that provides post-amplification and quantization. This circuit also includes a loss of signal detection circuit which provides an open collector logic high output in the absence of a usable input optical signal level or a disconnected/ broken fiber.

Serial Identification (EEPROM)
The HFBR-5701L and HFBR-5710L complies with an industry standard Multi-Source Agreement that defines the serial identification protocol. This protocol uses the 2-wire serial E2PROM protocol of the ATMEL AT24C01A or similar.

Table 1. HFBR-5701L/5710L Signaling Description

Pin	Name	Function/Description	Signal Level
1	VeeT	Transmitter Ground	
2	TX Fault	Transmitter Fault Indication - High Indicates a Fault	3.3 V LVTTL
3	TX Disable	Transmitter Disable - Module disables on high or open	3.3 V LVTTL
4	MOD-DEF2	Module Definition 2 - Two wire serial ID interface	3.3 V LVTTL
5	MOD-DEF1	Module Definition 1 - Two wire serial ID interface	3.3 V LVTTL
6	MOD-DEF0	Module Definition 0 - Grounded in module	
7	Rate Select	Not Connected	
8	LOS	Loss of Signal - High Indicates Loss of Signal	3.3 V LVTTL
9	VeeR	Receiver Ground	
10	VeeR	Receiver Ground	
11	VeeR	Receiver Ground	
12	RD-	Inverse Received Data Out	370 - 2000 mV differential (250 - 1200 mV single ended) [1]
13	RD+	Received Data Out	370 - 2000 mV differential (250 - 1200 mV single ended) [1]
14	VeeR	Receiver Ground	
15	VccR	Receiver Power	3.3 V ± 5%
16	VccT	Transmitter Power	3.3 V ± 5%
17	VeeT	Transmitter Ground	
18	TD+	Transmitter Data In	500 - 2400 mV differential (250 - 1200 mV single ended) [2]
19	TD-	Inverse Transmitter Data In	500 - 2400 mV differential (250 - 1200 mV single ended) [2]
20	VeeT	Transmitter Ground	

Notes:
(1) The typical receiver differential output voltage is 1500 mV to 50 Ohms with little variation.
(2) True differential, not single ended, voltage swings from 500 - 2000 mV are recommended for optimal performance.

2.2. HDMP-1687 Quad-SerDes

Description

The HDMP-1687 SerDes functional diagram is shown in Figure 2. It is a 1.25GBd GBE compliant SerDes with multi-rate capability and may in future offer compliance with other physical layer standards (e.g., 1.0625 Fibre Channel). The 10-bit wide parallel data lines support LVTTL signaling. For a more detailed description regarding the HDMP-1687, please visit the Agilent WebSite and look for the Product, Reliability, and Characterization Data Sheets which can be found in Reference 4.

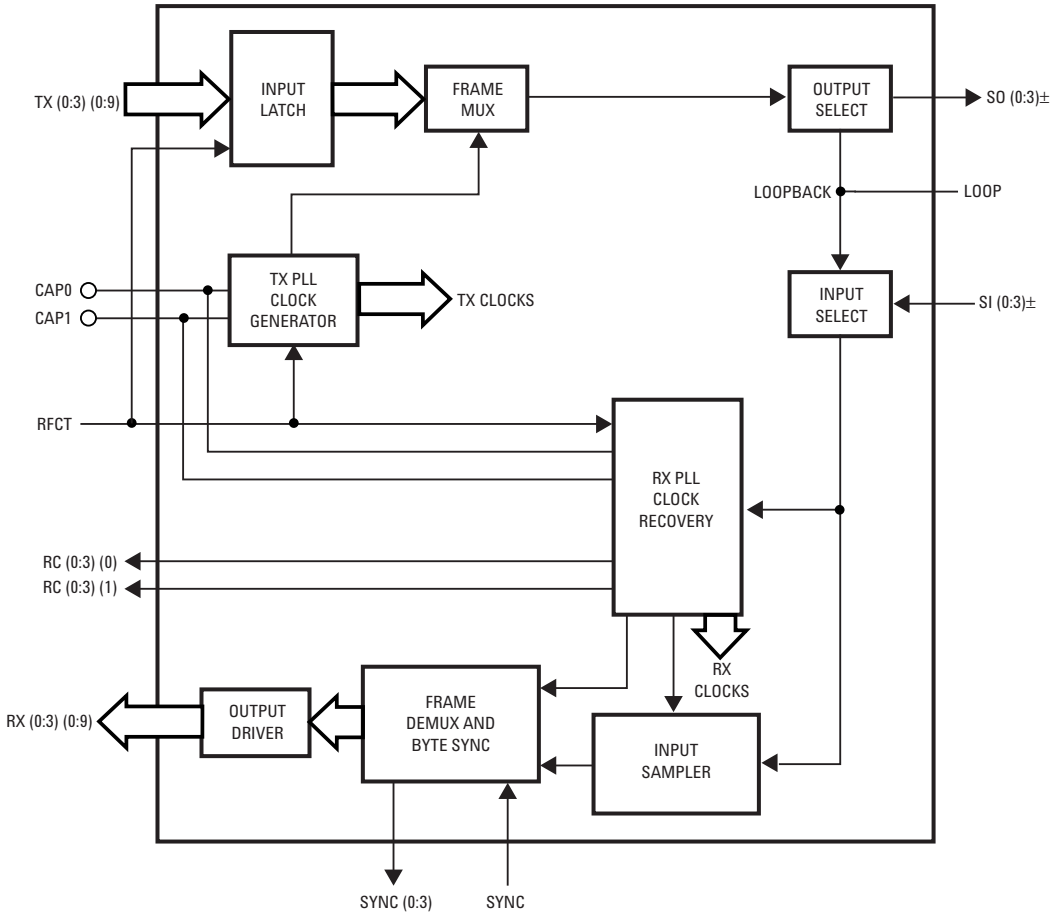


Figure 2. Functional Diagram of HDMP-1687

Table 2. HDMP-1687 Signaling Description

Name	Function/Description	Signal Level
SO(+/-)	Serial Transmitter Data Out (4 Channels)	1000 - 1800 mV differential
SI(+/-)	Serial Receiver Data In (4 Channels)	200 - 2000 mV differential
RX(0:9)	Parallel Receiver Data Out (10 lines on 4 Channels)	3.3 V LVTTL
TX(0:9)	Parallel Receiver Data In (10 lines on 4 Channels)	3.3 V LVTTL
RFCT	Receiver Frequency Reference Clock and Transmitter Byte Clock Input	3.3 V LVTTL
RCX(0:1)	Receive Byte Clock Output	3.3 V LVTTL
RCMO	RFCT Clock Rate Set (H-125 MHz, L-62.5 MHz)	3.3 V LVTTL
SYNX	Comma Detect Output (4 Channels)	3.3 V LVTTL
LOOP	HSIO Loopack Enable Input (H-EN L-DIS)	3.3 V LVTTL
SYNC	Enable Byte Synchronization Input (H-EN L-DIS)	3.3 V LVTTL

Section 3.

Detailed Description of the 1.25 GBd Reference Design Considerations

The reference design board shown in Figure 3 demonstrates the inter-operability of major components HFBR-5701L/5710L and HDMP-1687, their relevant data and control signal I/Os, power supply, and sampling points for both serial and parallel high speed signals. A detailed description can be found in Application Note 1242 in Reference 4.

3.1. Reference Design Guidelines and Printed Circuit Board (PCB) Layout Description

3.1.1. PCB Layer Stack-up

The reference design board consists of 12 primary layers: (1) Topside, (2) GND, (3) Signal, (4) Signal, (5) GND, (6) Signal, (7) PWR, (8) Signal, (9) GND, (10) Signal, (11) PWR, (12) Bottom-side. Layer (1) contains the footprints and control I/O signals for most of the reference design board's componentry including the SFP connector, the SFP cage, and the SerDes. Layer (12) contains the remainder of the passive components. Layers (3) and (4) contain the HSIO signal lines. Layers (3,4,6,8,10) contain the equal length parallel loopback lines for the SerDes. Layer (7) contains the VCC power supply for the SFPs and the SerDes with

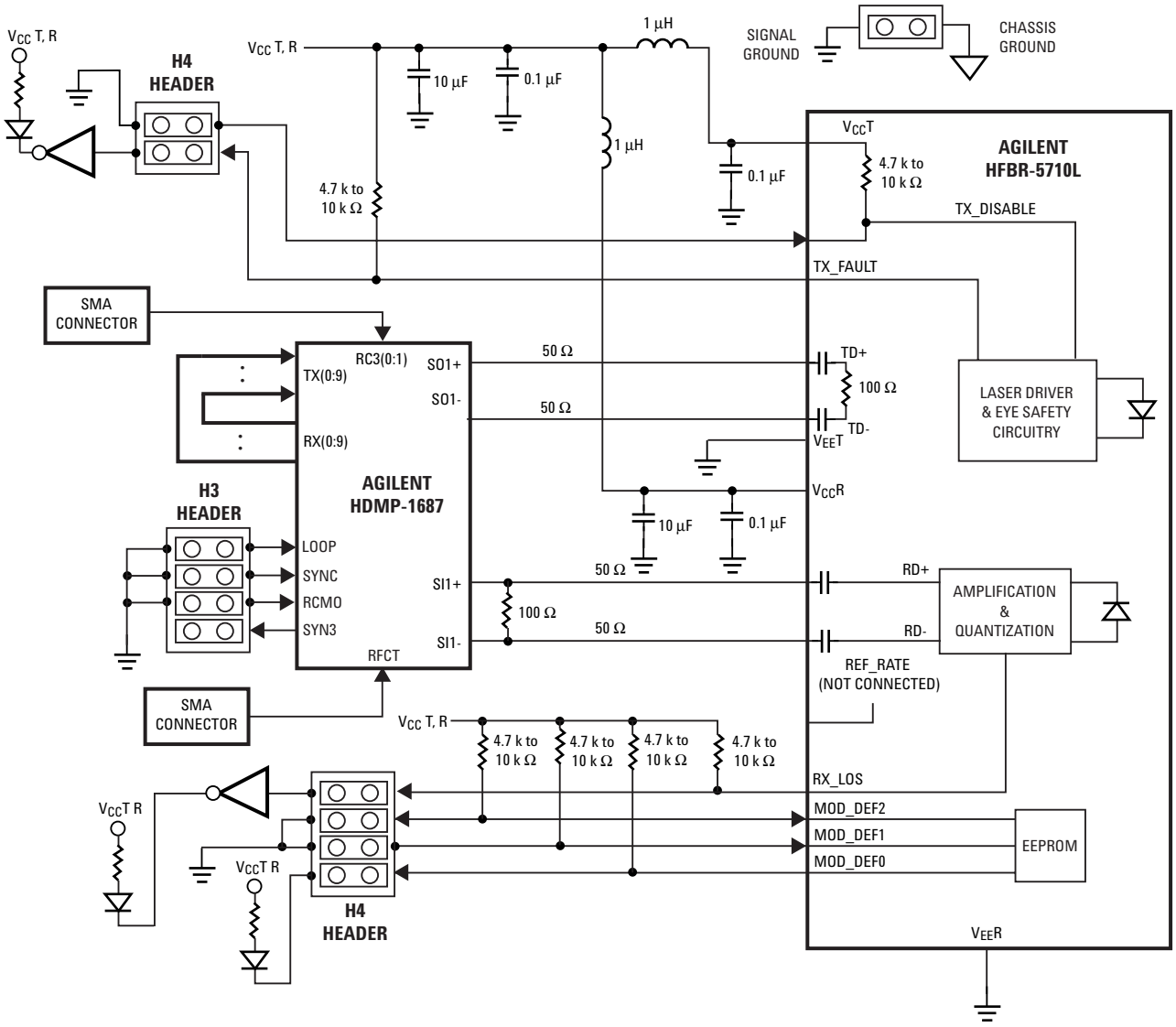


Figure 3. Reference Design Layout

the exception of the TTL I/O cells. Layer (8) contains a floating chassis ground for the SFP housing which is isolated from the SFP signal ground. Layer (11) contains the VCC_VCR power supply for the TTL I/O cells. The original artwork used to generate this board is available through your local Agilent Technologies representative.

3.1.2. "Belly-to-Belly Configuration."
Although not attempted for this reference design, the SFP MSA provides for modules to be mounted on both sides of a PCB with one SFP mounted in the mirror image of the other thus creating double density port counts. This is possible since the SFP MSA cage PCB pad arrangement is not symmetric. In order to address the mechanical de-latch issue that is created by mounting modules on both sides of the board, Agilent offers an extended de-latching mechanism which ensures that modules can be extracted one at a time without the use of special service tools. The extended de-latching feature is shown on the product data sheet for HFBR-5701L/5710L.

In order to address the thermal design considerations posed by this configuration, a belly-to-belly PCB was created and is discussed briefly in the thermal section of this application note. More detailed information regarding these technical issues may be available from Agilent Technologies to address this configuration, please contact your local representative.

3.1.3. SFP Cage and Connector
The MSA defined cage and surface mount connector detailed PCB footprints are shown in the product data sheet for HFBR-5701L/5710L. All mechanical details of the SFP can be found in the SFP MSA. The cage has little impact on HSIO, but it is one of the controlling factors for EMI which is described in more detail in the EMI section. The cage is the primary thermal path from the SFP to the outside air. It is also electrically isolated from the SFP signal ground for isolation from potentially large and random currents which may flow through an application box.

The SFP surface mount connector has been measured via a Differential TDR measurement revealing very little mismatch to the HSIO lines and differential 100 Ohm terminations internal to the SFP, thus good signal integrity can be achieved via proper transmission line design up to at least 2.125 GBd.

3.1.4. Special considerations for board layout
Routing High Speed I/O Lines
Due to the pin-out configurations of both the HFBR-5701L/5710L and the HDMP-1687, the HSIO transmission lines will have to cross one another as shown in Figure 4. This is true only when the SFP and SerDes are mounted on the same side of the board; however, this is not the case if they are mounted on opposite sides of the PCB.The number of intersections and the performance impact of each will depend upon the choice of transmission line geometry. Two common transmission lines that provide both signal integrity and EMI immunity are (1) broadside coupled striplines, and (2) edge coupled striplines.

Broad-side coupled striplines will minimize the number of intersections that have to be avoided by having transmission lines routed on multiple layers, but will maximize the PCB thickness which can lead to manufacturability concerns regarding details such as plating vias which must pass through all layers. Only intersections between pairs will have to be avoided (i.e., the differential pairs from the SFP RD(+/-) pins to the SerDes SI(+/-) will have to pass over or under the differential pairs SFP TD(+/-) pins to SerDes SO(+/-)). Intersections within differential pairs due to the relative orientation of RD(+/-) and SI(+/-) on the respective devices will not occur by definition since the differential pairs will already be on different vertical planes.

Edge coupled striplines will require the maximum number of intersections that have to be avoided, but they provide for the

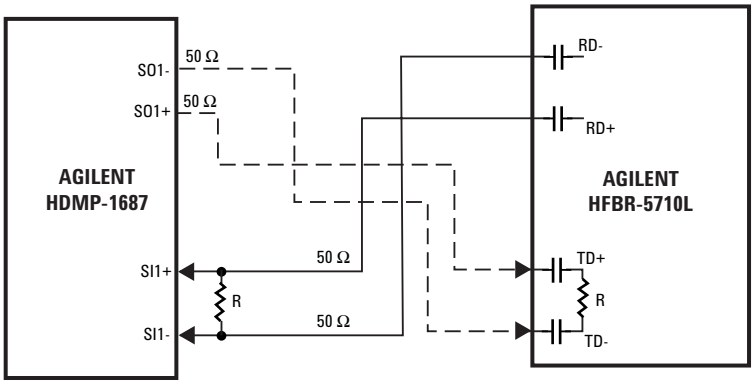


Figure 4. Edge Coupled Striplines Crossing One Another

minimum PCB thickness by minimizing the thickness required for a given layer achieve the appropriate impedance levels.

3.2. High Speed I/O Transmission Line Details

3.2.1. Terminations and Impedance Matching (e.g., AC Coupled, Value, Zo)
The HFBR-5701L/5710L are internally terminated, AC coupled, and DC biased internal to the module. The internal terminations are intended for differential signals with MSA compliant voltage swing (see Table 1) to terminate to 100 Ohms on the TD(+/-) pins. The effects of interfacing a 100 Ohm differential system to a 150 Ohm differential system (i.e., 75 Ohms single ended) are small and primarily consist of increased voltage swing at the load as shown in Figure 5. This figure shows simulated data of HDMP-1687 (modeled at 1600 mV differential drive) driving both a 150 Ohm (upper trace) and 100 Ohm (lower trace) differential load. Note that the ratio of the peak voltages (i.e., 1.8V/1.5V) is equal to 1.2 which is approximately equal to the expected value given a load with a voltage reflection coefficient of 0.2. This ratio would be 0.8 for the preceeding example if the transmission lines were 150 Ohms and the load was 100 Ohms.

Typically, LVPECL differential voltage swings will be on the order of 1600mV or less which is optimal for Agilent's SFPs. For TD (+/-) input voltage swings strictly greater than 2000 mV, voltage attenuation is preferred. A series resistor of anywhere from 10 to 15 Ohms may be used at the source end of the transmission lines to achieve the appropriate attentuation of voltage swing at the load. Given a differential voltage source of 2000 mV, the effects of varying a series resistor from 5 to 20 Ohms are shown in Figure 6. It can be seen that this effectively reduces the voltage swing at the load, to an acceptable level (e.g., <1600 mV), in proportion to the amount of voltage division between the series resistor and the load resistor. Typically, no external terminations, coupling capacitors, nor DC biasing need to be provided to the SFP module.

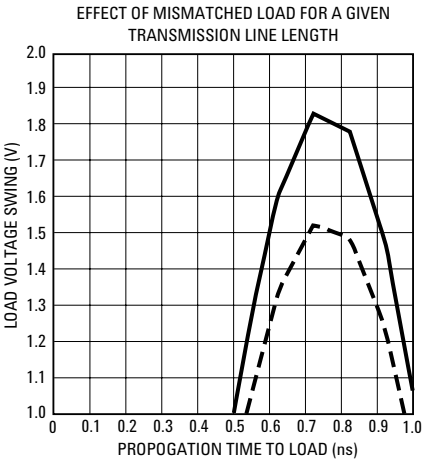


Figure 5. Effect on Peak Voltage at a Load by Varying the Load from 100 (Lower Trace) to 150 (Upper Trace) Ohms from a 100 Ohm System.

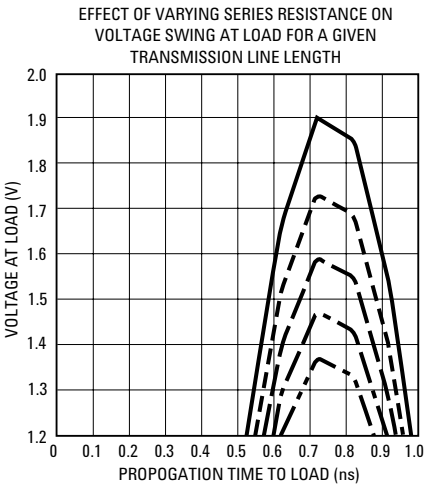


Figure 6. Effects of Varying a Series Resistor from 0.1 (Top Trace), 5.1, 10.1, 15.1, to 20.1 (Bottom Trace) Ohms on the Peak Voltage at a 100 Ohm Load from a 2000 mV Source

The HDMP-1687 does require an external termination of 2*Zo at its HSIO inputs (SI+/-). Otherwise, no external terminations, coupling capacitors, nor DC biasing needs to be provided to the HDMP-1687. As a result of this, the high speed signal transmission lines between RD(+/-) and SI (+/-) as well as between TD(+/-) and SO (+/-) can be directly connected after the appropriate choice of impedance levels and routing.

3.2.2. Recommended Transmission Lines and Characteristic Impedance
All things being equal, it is suggested that differential, coupled striplines be implemented to interconnect HSIO data signaling lines between the SFP and SerDes as shown in Figures 7 and/or 8 which are described in detail in Reference 5. Since they are surrounded by metal planes above and below, differential signal lines offer improved EMI generation and EMI susceptibility performance. These lines can be specified as 100 Ohms differential impedance and/or 50 Ohms Even (Zee) and 50 Odd Mode (Zoo) impedance as described in Reference 6. Weak Coupling between the pairs (e.g., <10 dB) ensures these impedance levels and minimizes the possibility of backward waves being launched as is the case in a directional coupler where line lengths greater than one half of a wavelength are present. However, care should be given to equilibrate the physical and electrical lengths of both pairs of high speed I/O lines to minimize skew between them which tends to suggest that the lines should be as close together as practicable without significantly increasing in coupling.

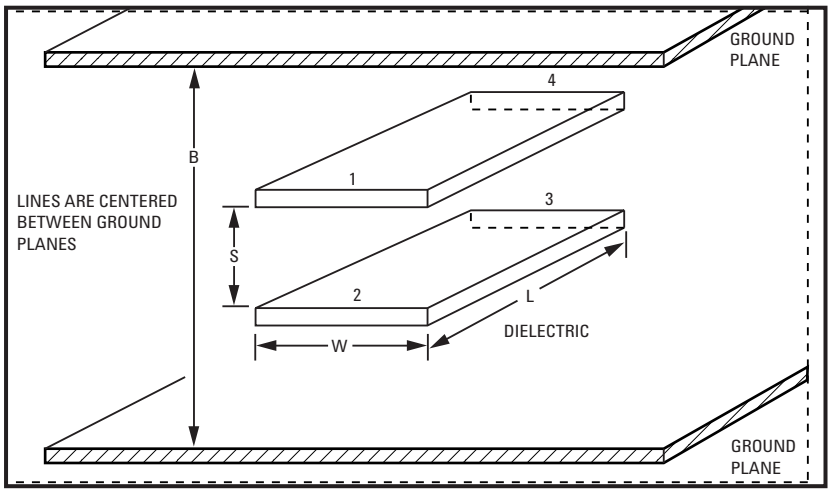


Figure 7. Broad-Side Coupled Striplines HSIO geometry

Table 3. Typical Broad-Side Coupled Stripline Values at 625 MHz (i.e., Clock Frequency Equivalent of 1.25 GBd)

W (mils)	S (mils)	L (mils)	B (mils)	T (mils)	Er	E_Eff (Deg)	Zoo	Zee	ZO
16	33	1000	75	0.7	4.4	40	49	69	58
9	18	1000	50	0.7	4.4	40	51	81	64
5.5	12.7	1000	25	0.7	4.4	40	46	58	52

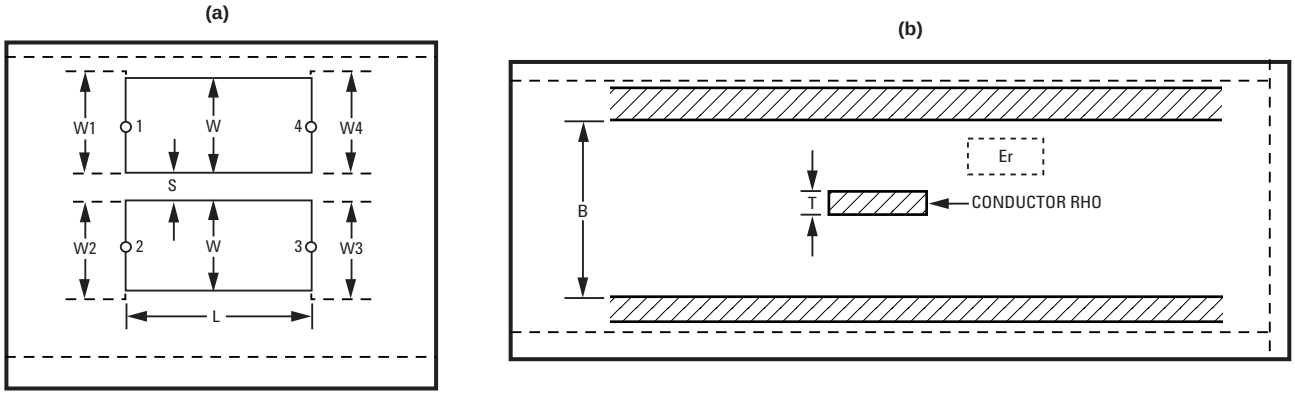


Figure 8. Edge-Coupled Stripline HSIO geometry (a) Top View, (b) Side View

Table 4. Typical Edge-Coupled Stripline Values at 625 MHz (i.e., Clock Frequency Equivalent of 1.25 GBd)

W (mils)	S (mils)	L (mils)	B (mils)	T (mils)	Er	E_Eff (Deg)	Zoo	Zee	ZO
8	20	1000	20	0.7	4.4	40	48	50	49
6	15	1000	15	0.7	4.4	40	47	49	48
4	10	1000	10	0.7	4.4	40	45	47	46

With frequencies in the 1 to 2 GHz range, line lengths of 2 inches or greater can equate to 90 degrees of electrical length or more. If there is an appreciable mismatch (e.g., VSWR >2:1) between the HSIO lines and the load impedance at the SerDes, it is possible to create the conditions for oscillation. This can be avoided by controlling the impedance of HSIO lines, minimizing vias, and keeping the spacing between the SerDes and the SFP as minimal as possible given the thermal conditions in the application which represents a fundamental trade-off. This has the added benefit of minimizing signal attenuation which can be on the order of 0.1 to 0.2 dB per inch.

3.2.3. IBIS Modeling
Agilent is in the process of developing Input/Output Buffer Information Specification (IBIS) for all relevant optical transceivers and SerDes ICs. IBIS models are time domain behavioral models that allow preliminary design simulation of high speed signal traces to assess the impacts of signal line lengths and impedance as described in Reference 8. An IBIS model for the HFBR-5701L/5710L may be available via the Agilent WebSite or by contacting your local sales representative.

3.3. Interpreting Jitter (Rj, Dj, and Tj)

Ever present in digital systems, jitter is a pervasive source of potential data errors and subsequent reduction in achieved bit error rate (BER). Jitter can be introduced by optical transceivers, SerDes, and system clocks among other sources. In this case, jitter generation is addressed; however, in general, jitter tolerance and transfer should also be considered. A definition of jitter is the displacement in time, from its ideal location, of the logic threshold (e.g., 50% amplitude crossing) for a data bit. The basic measure of jitter is the Unit Interval (UI). The UI represents the fraction of time that jitter displaces a data bit relative to the duration of a data bit, thus an 80 ps displacement of a data bit due to jitter would represent 0.1 UI for GBE which has data bit duration of 800 ps. The types of jitter that are generally quantified by measurement and specified in physical layer standards such as GBE include, but are not limited to, random jitter (Rj); deterministic jitter (Dj); and total jitter (Tj). A comprehensive background on jitter and its causes is beyond the scope of this application note, but a substantial amount of knowledge regarding the definitions, test methodologies, and specifications for jitter can be found in References 1,3, and 10. However, a basic understanding of each of these jitter components and an interpretation of them is addressed here in order to assist the reader in making these types of measurements and interpreting the data in the application note.

3.3.1. Random Jitter (Rj)
A basic definition of Rj is jitter that behaves as a statistical, random variable due to the nature of its source (e.g., thermal noise). The model for Rj contributed by electrical and electro-optical components used in this application note is the normal probability density function in time with non-zero standard deviation, $\sqrt{(\sigma)^2}$ and zero mean μ.

Typically, both peak to peak and one standard deviation values for Rj can be measured on a digital sampling oscilloscope or digital communications analyzer using a repeating K28.7 (1100000111) pattern and monitoring the 50% data amplitude crossing point. This repeating pattern is balanced in time so that the effects of pattern dependency on the measurement are minimized. This method is limited in its ability to measure peak to peak Rj, and Tj for that matter, due to limitations on the number of triggering events and the amount of data which can be stored. This is one reason for measuring the standard deviation for Rj instead of its peak to peak value.

For comparison with both GBE and FC specifications, the preferred interpretation of Rj is to convert the measured standard deviation, $\sqrt{(\sigma)^2}$, to a peak to peak value by calculating Rj(pp) via Equation 1. The number 14 is derived from the area under the normal distribution curve that equates to a BER of $1x10^{-12}$. In other words, with a standard deviation of $\sqrt{(\sigma)^2}$, 99.9999999999% of the possible values for Rj are contained in a time interval of $-7 * \sqrt{(\sigma)^2}$ to $+7 * \sqrt{(\sigma)^2}$ or an area under the curve that leaves only a 1 in 10^{+12} possibility that the value of Rj could reside outside of this range and cause a bit error.

Equation 1. Calculation of Peak to Peak Random Jitter Rj(pp) from its Measured Standard Deviation

[1] $$Rj(pp) = 14 * \sqrt{(\sigma)^2}$$

Since we are treating Rj as a normally distributed, random variable with a standard deviation of $\sqrt{(\sigma)^2}$ then the rules of addition of random variables apply in that their variances, $(\sigma)^2$, are additive. For example, if we want to calculate $\sqrt{(\sigma_3)^2}$ at the output of and electro-optical device given that $\sqrt{(\sigma_1)^2}$ is present at its input and its contributed Rj is known to

be $\sqrt{(\sigma_2)^2}$, then we simply solve Equation 2.

Equation 2. Calculation of Rj at the Output of an Electro-Optical Device with Known Input and Contributed Rj

[2] $(\sigma_3)^2 = (\sigma_1)^2 + (\sigma_2)^2$

Another important case, Equation 3, is if we want to calculate the amount of Rj that an electro-optical device can contribute, $\sqrt{(\sigma_2)^2}$, given that $\sqrt{(\sigma_1)^2}$ is specified its input and $\sqrt{(\sigma_3)^2}$ is specified at its output. This is typically the case when deriving the allowable Rj contribution for an optical transceiver between two specified compliance points in a physical layer standard such as GBE (e.g., TP1 and TP2) or FC-PI.

Equation 3. Calculation of Allowable Contributed Rj by an Electro-Optical Device with Known Input and Output Rj Limits (e.g., GBE or FC specifications)

[3] $\sqrt{(\sigma_2)^2} = \sqrt{[(\sigma_3)^2 - (\sigma_1)^2]}$

3.2.2. Deterministic Jitter (Dj)
A basic definition of DJ is jitter that behaves predictably or repeatably. Dj sources include pattern dependency and/or duty-cycle distortion among others. The model for Dj contributed by electrical and electro-optical components used in this application note is that Dj adds linearly as in Equation 4. The allowable contributed Dj by an electro-optical device can be derived directly by re-arrangement of Equation 4.

Typically, peak to peak Dj can be measured on a digital sampling oscilloscope or digital communications analyzer in a waveform averaging mode using a repeating K28.5+/- (1100000101, 0011111010) pattern and monitoring the 50% data amplitude crossing points. The range of the deviations in time of the 10 logic transitions (i.e., 1 to 0 and 0 to 1) present in this 20 bit pattern from their ideal locations in time represents one method for quantifying Dj. This repeating pattern is used because it contains the longest allowable data sequence for valid 8B10B coding (i.e., 5 data bits) as well as the shortest data sequences 010 and 101. It is heavily averaged over many waveforms to remove any contribution due to random jitter.

Equation 4. Calculation of Dj at the Output (Dj_3) of an Electro-Optical Device with Known Input (Dj_1) and Contributed (Dj_2)

[4] $Dj_3 = Dj_1 + Dj_2$

3.2.3. Total Jitter (Tj)
Total jitter (Tj) can be considered the sum of all sources of jitter such as Rj and Dj independently affecting a data bit sequence. Tj is the most important jitter variable to quantify since it is actually the one that is present in the system. Tj budgeting is done in both GBE and FC-PI by estimating Tj at one end of the physical layer and budgeting it at intermediate reference planes or compliance points all of the way to the other end of the physical layer. The absolute limits on Tj are derived by specifying a minimum allowable received eye-opening (i.e., un-affected by jitter and of sufficient amplitude) of a data signal having traversed the entire physical layer. Tj is specified as a peak to peak value and it is the amount that an ideal eye-opening can be reduced such that the remainder, the eye-opening, meets the specified BER as presented to a SerDes or data recovery device.

Tj can be measured, and is suggested to be in most standards, by a bit error rate tester (BERT) used to measure the eye-opening yielding the required BER from which Rj and Dj can be estimated. An alternate and informative method is to measure Dj and Rj by the aforementioned methods and to calculate Tj as in Equation 5. Both of these methods model the Tj as a random variable with a mean of μ = Dj and standard deviation of $\sqrt{(\sigma)^2}$ = Rj.

Equation 5. Calculation of Peak to Peak Value of Tj at a Compliance Point Given Rj and Dj Have Been Measured

[5] $Tj = Dj + Rj(pp)$

Typically Tj and Dj, but not Rj are specified in standards such as GBE at input and output compliance points as well as the electro-optical device contribution between them. It is usually stated that the Rj contributed by a device can vary as long as the sum of Rj(pp) and the specified value of Dj does not exceed the specified value of Tj at an output compliance point (e.g. TP2) given the Tj at an input compliance point (e.g., TP1). It is important to note that the calculation of Tj contributed by an electro-optic device is complicated by the nature of Equations 3 and 4. As a result, device contributed Tj is not simply the linear subtraction of the allowable Tj at the device output and the allowable Tj at the device input specified by the appropriate compliance points. In fact, the allowable contributed Tj

will vary as the sum of Rj and Dj vary with a maximum value at Dj = 0 and Rj = Rj(max) and a minimum value at Dj = Dj(max) and Rj = 0. Typically, the standards will specify a value of Tj contributed by specifying an intermediate value of DJ contributed. For GBE, this value if Dj=80 ps (0.1 UI).

For example, from the GBE specification, the total allowable contributed Tj between compliance points TP1 and TP2 is 227 ps which is not equal to the linear subtraction of the absolute values of allowable Tj at TP2 and TP1 which is to only 153 ps. This is because the contributed value of Tj is made up of a contributed DJ of 80 ps and a contributed Rj(pp) 147 ps which is calculated by use of Equation 3. In fact, the values of contributed Dj and Rj between compliance points TP1 and TP2 can vary significantly while still meeting the allowable value of contributed Tj for the device. At one extreme, Tj can decrease to a limiting minimum value equal to a linear subtraction of the allowable contributed Tj between TP2 and TP1 of approximately 153 ps with an assumed contributed Rj(pp) of zero and a maximum Dj contribution equal to the total Tj contribution. At the other extreme, contributed Tj can increase to a maximum limiting value composed entirely of contributed Rj(pp) equal to approximately 240.2 ps with a minimum contributed Dj value of zero (theoretically it can be negative, but not practically). This trade-off between contributed Rj(pp) and contributed Dj between TP1 and TP2 of the GBE standard is shown graphically in Figure 9.

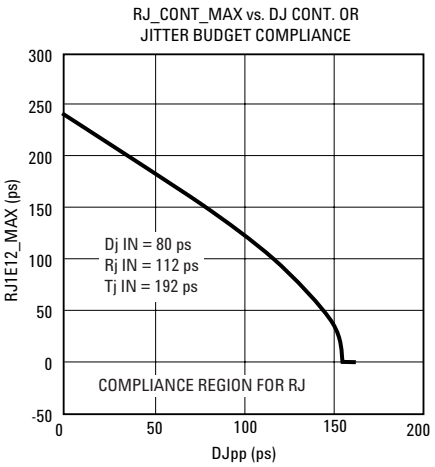


Figure 9. Range of Values for Contributed Dj and Rj(pp) Meeting Contributed Tj for GBE at TP2 Given TP1 per the Standard

3.4. Multi-Rate (1.25/1.0625) Compatibility

The reference design supports operation at both 1.25 GBd and 1.0625 GBd. The dual rate operation of the HFBR-5701L is assured simply by virtue of its wide instantaneous receive bandwidth for both GBE and FC applications. The HDMP-1687 may support multi-rate capability in the future as well, please contact your local Agilent sales representative for details.

An electrical filter is implemented after the receiver's PIN photodiode which serves to reject high frequency noise outside of the desired signal pass-band of interest. For test purposes, this filter is specified as a Fourth Order Bessel-Thompson low pass filter whose amplitude response Equation 6. For 1.25 GBd operation, the 3dB frequency is ideally 937 MHz whereas for 1.0625 GBd operation, the 3dB frequency is ideally 800 MHz. Both GBE and FC-PI specify an upper limit of 1500 MHz for this parameter.

The Fourth Order Bessel-Thompson Low Pass filter amplitude response is plotted versus frequency in Figure 10 for both 800 MHz and 1500 MHz filters. In addition, the group delay response is plotted for both filter options in Figure 10. It is the flat group delay response which leads to the choice of the Bessel-Thompson filter over other options such as Butterworth, Chebyshev, Elliptical, etc ... . This filter response maximizes linearity or a true time delay while minimizing dispersion by implementing a flat group delay response.

One interoperability issue that arises with the wider filter bandwidth operation is the possibility that signal frequencies from legacy laser products which were intended for use with 1.0625 GBd receivers will have unwanted frequency content in the pass-

Equation 6. 4th Order Bessel-Thompson Filter Response

$$H_P = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4}$$

With

$$y = 2.114p \qquad p = \frac{j\omega}{\omega_r} \qquad \omega_r = 2\pi f_r \qquad f_r = 0.75\text{xBit rate}$$

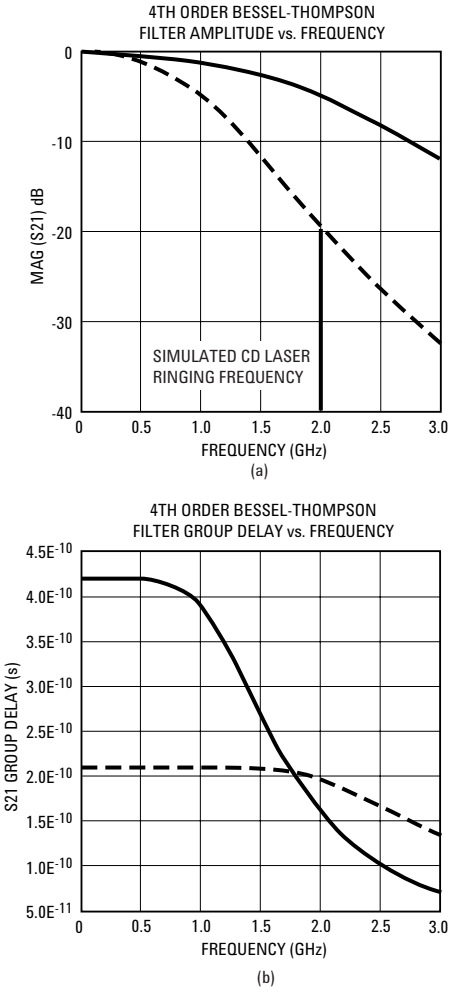


Figure 10. 4th Order Bessel-Thompson Filter Response (A) Amplitude (CD Laser Frequency Shown), (B) Group Delay

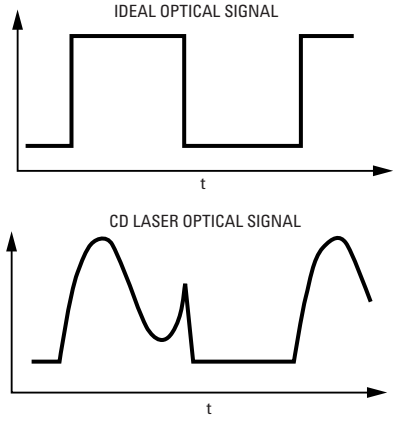


Figure 11. Legacy CD Laser Signal versus Ideal Optical Signal

band of the wider filter. For example, Compact Disc (CD) laser products may exhibit "ringing" as shown in figure 11. This ringing in the optical domain may cause unwanted frequency content within the pass-band of a wider bandwidth receiver filter which would be filtered out by a true 1.0625 GBd filter as simulated in Figure 10(A).

3.5. Electromagnetic Interference (EMI) Emissions

3.5.1. Cage and Chassis Considerations

Every system sold in the US or Europe is subject to Electromagnetic Interference (EMI) controls enforced FCC or CISPR requirements for un-intentional radiators. Since the SFP modules protrude through the chassis, they are a likely location for either generating EMI or leaking EMI from within the application. This is particularly a concern for pluggable modules where the SFP to EMI cage interface are now system variables. Various Agilent Application Notes and White Papers provide detailed descriptions of EMI basics, requirements, and design considerations for meeting FCC and CISPR EMI levels. These can be found in Reference 4.

The SFP MSA cage is shown on the reference design board on the front cover of this document. It is two pieces with the bottom half soldered to the host PCB via through hole pins. An alternate cage version has press-fit pins on the bottom half. This version has the potential advantages of automated assembly and enabling the belly-to-belly configuration.

The SFP MSA standard bezel opening for the host chassis is shown in Figure 12 from Reference 7. The contact between the SFP cage and bezel opening as well as that between the SFP module and the SFP cage are the strongest determinants of EMI performance at the system level. Ensuring proper SFP insertion, including sheer pin contact to the cage, will minimize the possibility of a loud module dominating the performance of an otherwise quiet system.

3.6.1. SFP EMI Goals

Agilent's SFP was designed for port counts as high as 100 modules at FCC B levels noting that successful application EMI certification is always a function of both the SFPs and the quality of the application chassis. From the system level goal, module level EMI criteria are developed. The GigaHertz Transverse

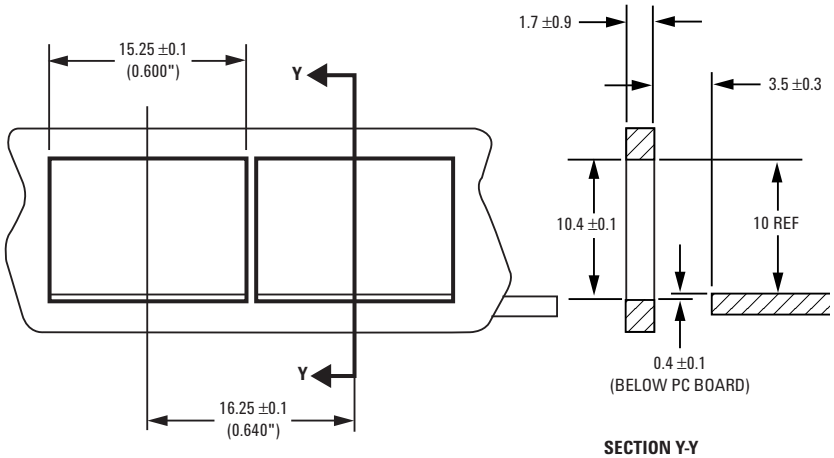


Figure 12. SFP MSA Standard Chassis Bezel Opening

Electromagnetic (GTEM) Test Facility is used to screen SFP modules for EMI performance. This is how Agilent's EMI mitigation techniques are built into the SFP and verified so that applications will not have to add-on EMI mitigation later. Typically, a 20 bit GBE idle pattern such as K28.5, D16.2 (1100000101,0110110101); the 40 bit Fibre Channel Idle pattern such as K28.5, D21.4, D21.5, D21.5 (0011111010, 1010100010, 1010101010, 1010101010); and/or a square-wave (10) pattern will be used to test EMI on individual modules as appropriate. The effects of varying the GBE idle pattern, which is allowable via that specification, have been investigated and are documented in Reference 8.

3.6. Thermal Considerations: Case Temperature, Ambient Temperature, and Reliability

In any application, there are two distinct temperature boundaries (1) 0-70°C, (2) 85°C that have specific implications for performance and reliability of the HFBR-5701L/5710L which are noted in the product data sheet and reliability data sheet.

Between 0 and 70°C, the SFP has been characterized for performance relative to GBE, FC-PI, or both to ensure conformance to the product data sheets. High temperature operating life (HTOL) or accelerated life testing of 55 SFP modules has been performed at 85C for over 88,000 hours. This yields an accelerated total equivalent of 161,797 hours at 70°C which is used to establish a predicted point MTTF of 18.5 years, 8 years with a 90% confidence interval, and/or 20.2 years with a 60% confidence interval.

At 85°C, the absolute maximum value for case temperature of the SFP is reached. From 70°C up to and including 85°C, the performance of the SFP is ensured by virtue of the HTOL testing. At temperature above this, the SFP may not function to data sheet limits and damage to the device may occur.

The referenced temperatures for HTOL testing are all ambient temperatures measured in the immediate vicinity of the SFP module thus the equivalent case temperature may in fact be several degrees higher. The reference point for the case temperature is measured at the center of the module LC-connector as shown on the product data sheet. More detailed information can be found at Reference 4.

While there is no specific environmental specification for GBE or FC applications, in the telecommunications market, the Network Equipment Building System Standard, GR-63 (Reference 9) has been developed. This document clearly defines applicable environmental conditions, typical applications are specified for room environments of 0-50°C room temperatures. For an assumed room temperature of approximately 30°C, an estimated 10°C additional ambient temperature rise in the application box, so that SFP ambient temperatures start at approximately 40°C. A row of 20 SFP modules with the SFP MSA minimum spacing as in Figure 12, subjected to 1.0 m/s airflow may see an additional temperature rise of 10°C which results in an operating case temperature of 50°C at the most susceptible SFP in the row. This can easily be exceeded with improper airflow or board layout since the surrounding components (e.g., SerDes) also can heat the SFPs. In designing an application box, specific MTTF goals for SFPs should be developed and the thermal flow conditions to meet these should be generated. The relibility implications of the SFP case temperature for random failures can be found in the reliablility data sheet. Reliability data for Agilent's VCSEL which may deviate from the MTTF data can be found by contacting Agilent.

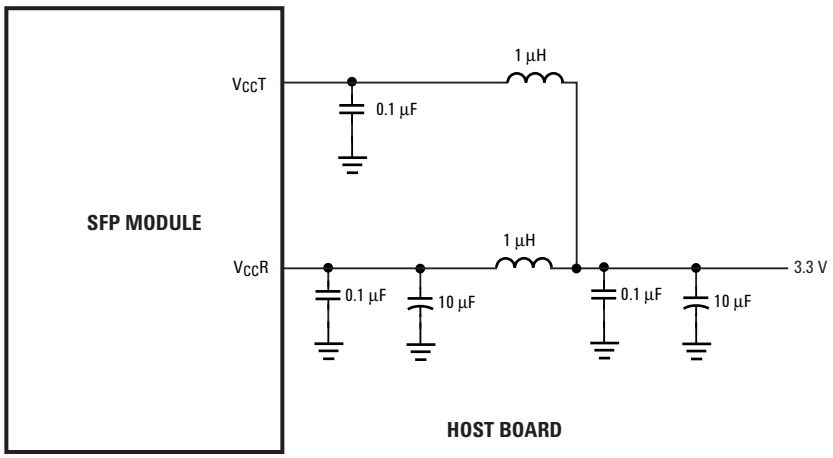


Figure 13. Required SFP MSA Host PCB Filter

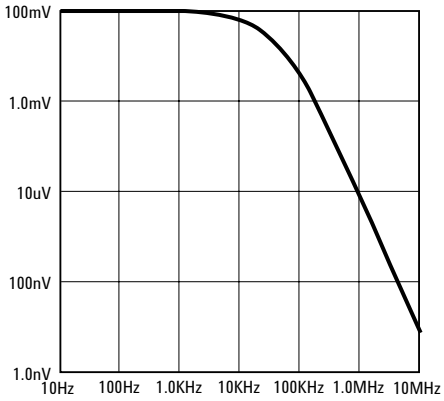


Figure 14. Typical Frequency Response of the Required SFP MSA Host PCB Filter

3.7. Power Supply Noise Issues

3.7.1. Required Filtering for SFP and SerDes

The required SerDes power supply filtering consists almost exclusively of 0.1 micro-farad high frequency by-pass capacitors with the exceptions of the SerDes Phase Locked Loop (PLL) pins. These filters are implemented with PSN filtering via single section L-C filters or the equivalent of the SFP MSA filter. The Product Data Sheet for HDMP-1687 gives specific details for the placement and values of these components.

The SFP MSA specifies a power supply filter which is shown in Figure 13. This filter is required on the host board when using HFBR-5701L/5710L. This filter services both power supply filter requirements and hot-plugging (a.k.a. “in-rush”) requirements. The typical frequency characteristic of the SFP MSA filter is shown in Figure 14 in response to an assumed 100 mVpp AC swept signal. This is commensurate with the noise that can be present on systems utilizing switching power supplies.

3.7.2. Power Supply Noise System Impacts

There are several measurable effects that result from the presence of Power Supply Noise (PSN). With a simulated 100 mVpp AC noise applied and swept from 10 Hz to 1 MHz the following parameters are typical pass fail criteria: (1) SFP transmitter eye diagram mask margin reduction less than 10%, and (2) SFP receiver sensitivity reduction less than 1 dB. The transmitter eye diagram mask margin reduction also manifests itself as reduced eye-opening for a given bit error rate which can have a much larger system level impact by reducing the systems tolerance to jitter.

3.7.3. Hot-Plugging

The SFP filter serves the dual purpose of supplying the in-rush current to the SFP, charging it’s internal PCB bypass capacitors, as well as power supply filtering. In particular, the 10 micro-farad capacitors should be implemented to mitigate any transient voltage droop at the SFP during hot-plugging. This ensures that adjacent parts are un-affected by hot-plugging events.

Electro-Static Discharge (ESD) effects have also been tested and all regulatory tests have been passed. It is useful to note that the EMI Cage Ground (i.e., Chassis Ground) and the SFP Ground (i.e., Signal Ground) are distinct from one another when using Agilent's SFP.

The SFP MSA specifies the successful completion of 100 hot-plug insertion cycles to ensure mechanical integrity. Agilent's SFPs meet this as well as hot-plug insertion and operational initialization over temperature (0 to 70°C) and voltage supply variation (3.3 V +/- 5%).

Section 4.

Reference Design Board Test Results

Testing utilizing the evaluation and reference design PCBs was conducted for typical IEEE 802.3 compatibility at test points TP1, TP2, and TP4. The physical layer eye-diagram performance was evaluated by testing for eye mask margin, extinction ratio, eye-height, eye-width, rise-time, fall-time, BER, et. al, the results of which are summarized in Table 5. In addition, the physical layer jitter performance was evaluated by testing for Random Jitter (RJ), Deterministic Jitter (DJ), Total Jitter(TJ), and Eye-Opening versus BER the results of which are summarized in Table 6. The basic test configuration is shown in Appendix A along with a definition of the test sampling points. A more detailed description of the testing methodologies implemented can be found in References 1,3, and 10.

1.25 GBd Optical and Electrical Test Results

Table 5. Summary of Test Results for Configuration A with 1 M of 50/125 micron Optical Fiber

	ER (dB) [1]	Rise Time (ps) [2]	Fall Time (ps) [2]	Eye Height (μW) [1]	Eye Width (ps) [1]	Mask Margin (%) [1]	Vo (mVpp)	BER Meas.
TPA	14.24	168	199	541.8	693.4	44		
TPB	14.24	168	199	545.54	692.5	49		
TPC	14.35	170	200	548.05	696.1	50		
TPD	14.3	169	200	556.56	688.9	48		
TPE	13.73	210	228	418.3	732.7	57		
TPF		182	195					
TPG		106	110				809	
GBE or MSA Spec.	9	260	260			>0	187.5 - 1000	$< 10^{-12}$
RESULT	✓	✓	✓	N/A	N/A	✓	✓	✓

Notes: (1) Measured with PRBS 2^7-1 Pattern Applied at 1.25 GBd (see Figures 15 and 16).
(2) Measured with K28.7 pattern and 4th Order Bessel-Thomson filter (see Figures 19 through 23).

Table 6. Summary of Test Results for Configuration A with 1 M of 50/125 micron Optical Fiber

	Total Rj Meas. (ps-rms)	ΔRj[1] Meas. (ps-rms)	Total Dj Meas. (ps-pp)	ΔDj[2] Meas. (ps-pp)	Total[5] Jitter Calc. (ps-pp)	RJ[3] Calc. (ps-rms)	DJ[4] Calc. (ps-pp)	TJ[5] Calc. (ps-pp)	Eye Open @ 10^{-5} BER (ps-pp)	Eye Open @ 10^{-9} BER (ps-pp)	Eye Open @ 10^{-12} BER (ps-pp)
TPA	14.79	8.4	83	64	284.06						
TPB	14.83	8.5	77	59	282.62						
TPC	14.58	8.1	75	67	284.12						
TPD	14.86	8.5	80	57	279.04						
TPE	6.51	6.02	71	54	172.32						
TPF	14.59		32			13.01	36.93	219.01	652	607	581
TPF (loopback)	5.02										
TPG	12.15		20								
GBE or MSA Spec		10.35	160	80	345	16.35	370	599	>202	>202	>202
RESULT	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes:
(1) Contributed Rj corrected for Rj at TPG see Equation 3 and measured with K28.7 pattern see Figure 23.
(2) Contributed Dj corrected for DJ at TPG see Equation 4 and measured with K28.5 pattern see Figure 24.
(3) RJ=0.5(T1-T0)/(Q1-Q0) per References 1, 3.
(4) DJ=[UI-T0-(2xQ0xRJ) per References 1, 3.
(5) TJ=DJ+14 • RJ see Equation 5.
(6) Standard test procedure calls for measurement at sensitivity + 0.5 dB and stressed receiver pattern.

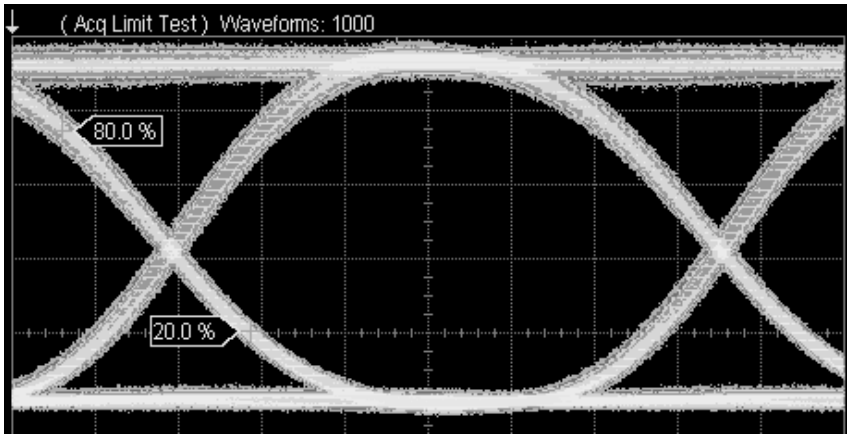


Figure 15. Optical Test Point TPE (Evaluation PCB) Eye Pattern with PRBS 2^7-1 Pattern Applied

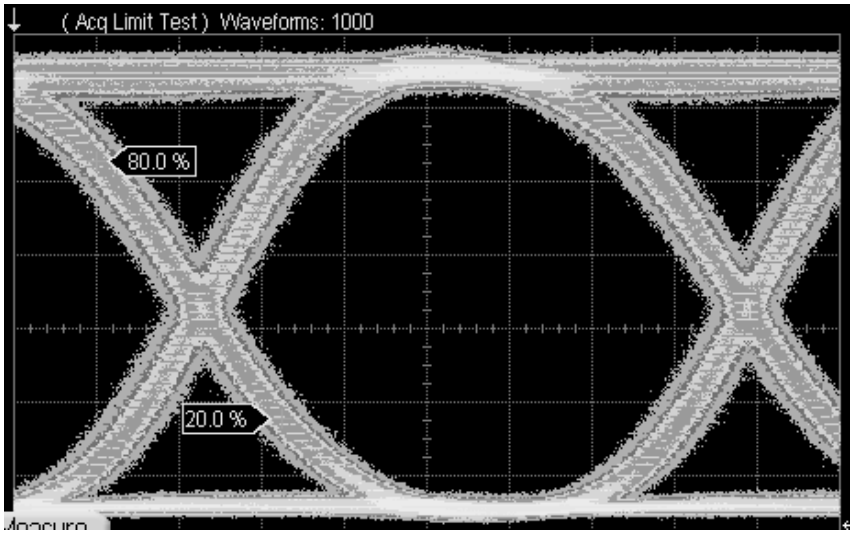


Figure 16. Optical Test Point TPA (Reference Design PCB) Eye Pattern with PRBS 2^7-1 Pattern Applied (Data is representative of performance on all four channels)

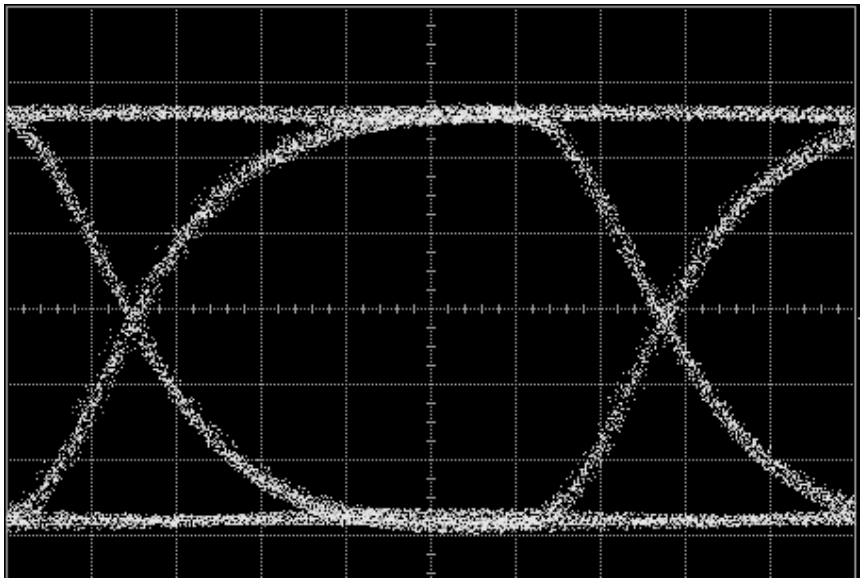


Figure 17. Electrical Test Point TPF (Evaluation PCB) Eye Pattern with PRBS 2^7-1 Pattern Applied in Self-LoopBack Configuration (TPE, TPF)

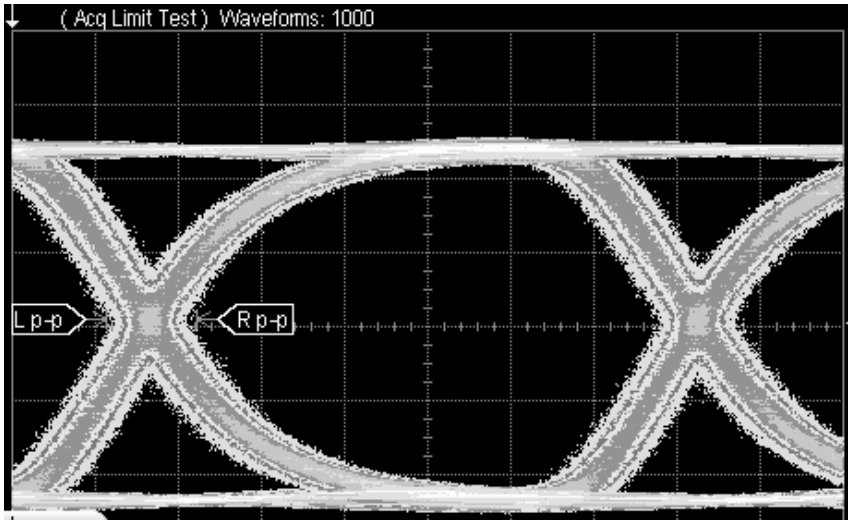


Figure 18. Electrical Test Point TPF (Reference Design PCB) Eye Pattern with PRBS 2^7-1 Pattern Applied in LoopBack Configuration (TPE, TPA, TPF) (Data is representative of performance on all four channels)

(a) (b)

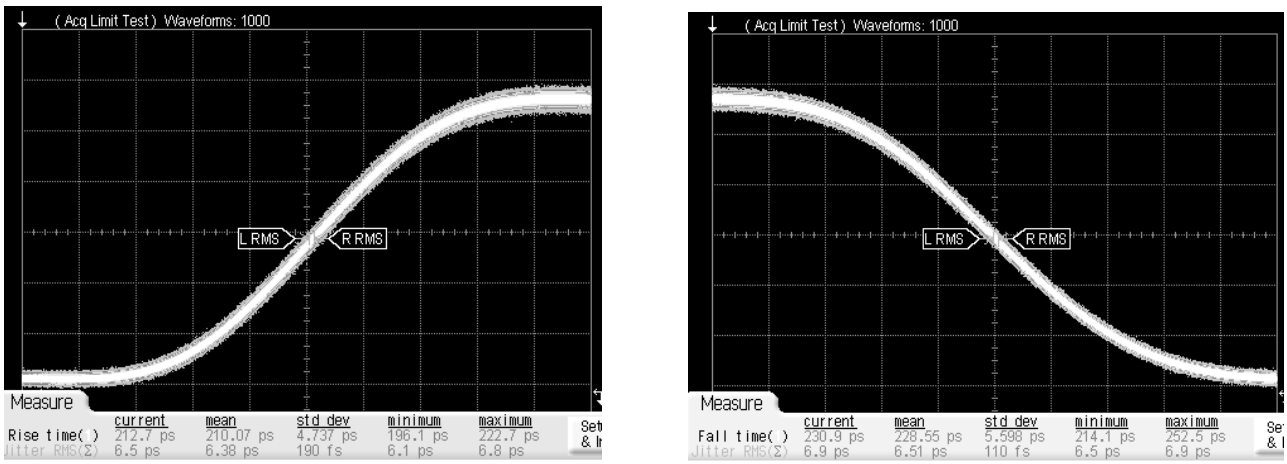


Figure 19. Optical Test Point TPE (Evaluation PCB) (a) Rise Time and (b) Fall Time with K28.7 Pattern Applied

(a) (b)

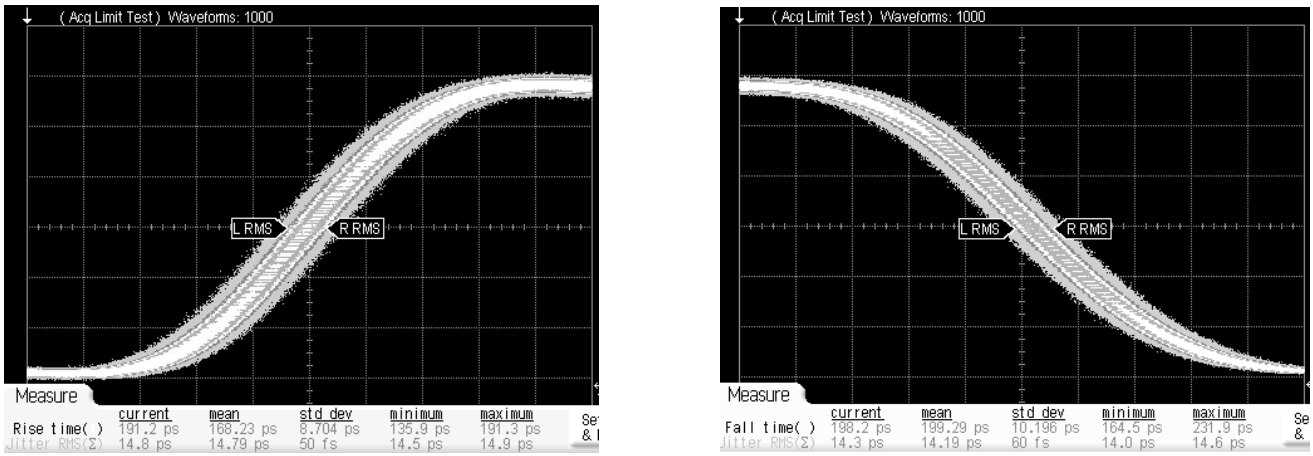
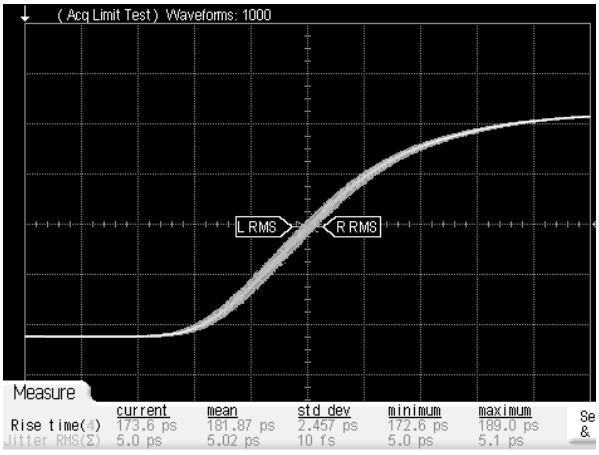


Figure 20. Optical Test Point TPA (Reference Design PCB) (a) Rise Time and (b) Fall Time with K28.7 Pattern Applied (Data is representative of performance on all four channels)

(a)



(b)

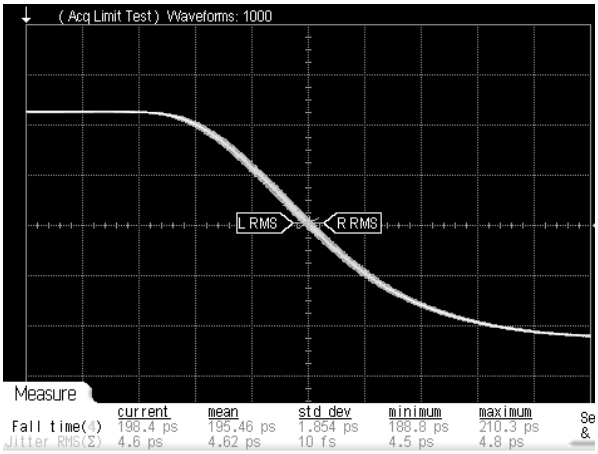
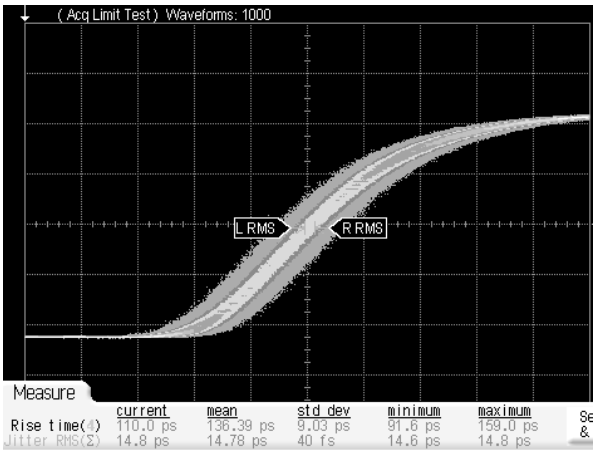


Figure 21. Optical Test Point TPF (Evaluation PCB) (a) Rise Time and (b) Fall Time with K28.7 Pattern Applied in a Self-Loopback Configuration (TPE, TPF)

(a)



(b)

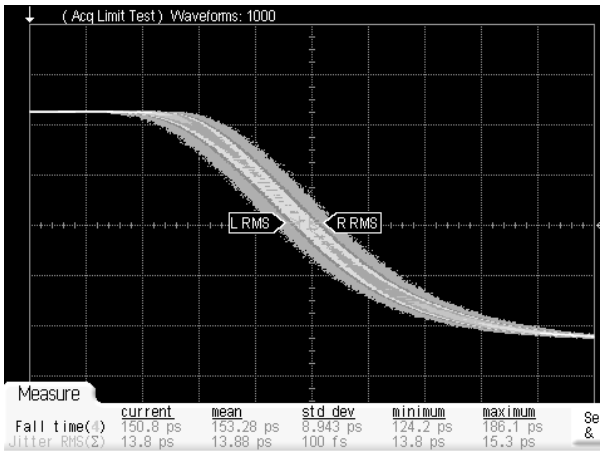


Figure 22. Optical Test Point TPF (Evaluation PCB) (a) Rise Time and (b) Fall Time with K28.7 Pattern Applied in a Loopback Configuration Through the Entire Physical Layer (i.e., TPE, TPA, TPF) (Data is representative of perforFmance on all four channels)

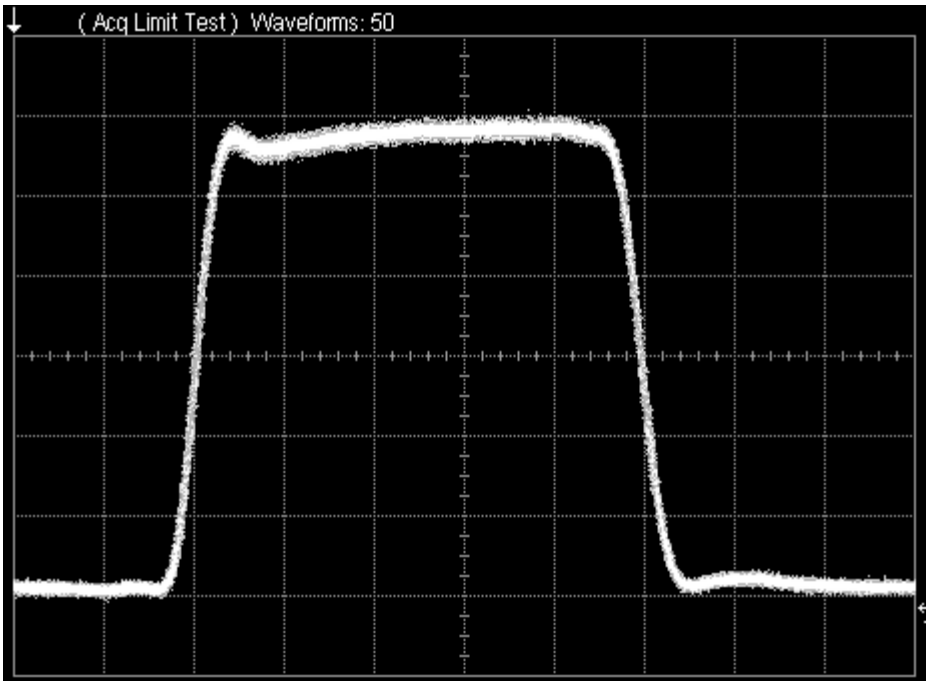


Figure 23. Optical Test Point TPE (Evaluation PCB) RJ with K28.7 Pattern Applied

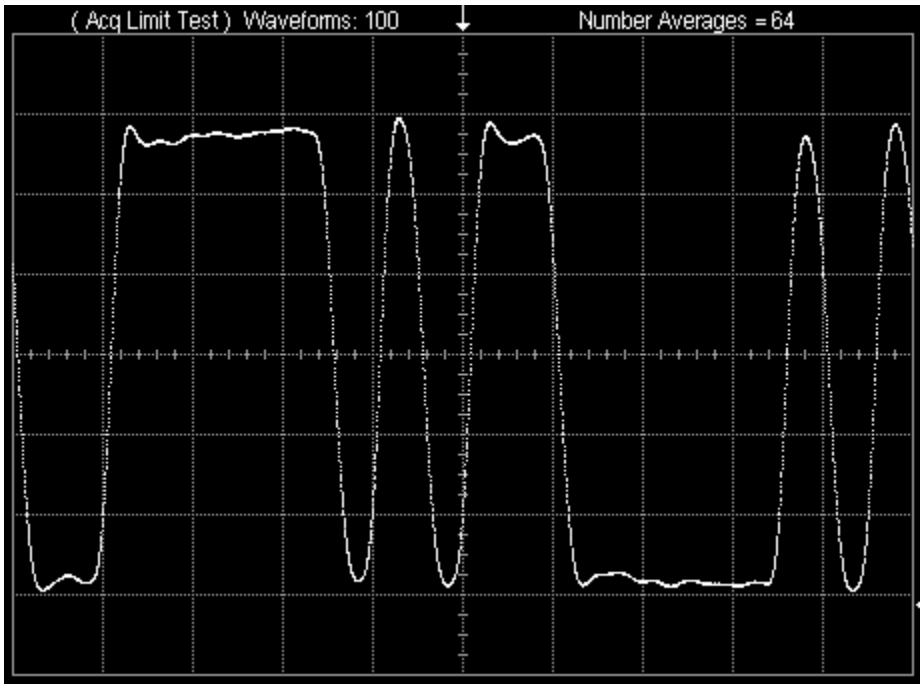


Figure 24. Optical Test Point TPE (Evaluation PCB) DJ with K28.5 Pattern Applied

Section 5.
Conclusions and Recommendations

1. Technical Issues Addressed

- SFP/SerDes Physical Layer Reference Design Description, Design Criteria, and Printed Circuit Board (PCB) Layout Description
- High Speed Input/Output (I/O)
- Interpreting Jitter (Rj, Dj, and Tj)
- Multi-Rate Compatibility (1.25 GBd and 1.0625 GBd)
- Electromagnetic Interference (EMI)
- Thermal Design Considerations
- Power Supply Noise Rejection

2. 1.25 GBd GigaBit Ethernet physical layer solution is available from Agilent Technologies.

This solution consists of the HFBR-5701L/5710L Small Form-factor Pluggable (SFP) optical transceiver and the HDMP-1687 Quad-Channel SerDes. These part are shipping summer 2001 so contact your local Agilent sales representative today!

3. For More Information Please Contact:

Your Local Agilent Sales Representative or the Agilent WebSite at "www.semiconductor.agilent.com"

Section 6.
References

1. GigaBit Ethernet Specifications
IEEE 802.3 2000 Edition
URL - http://www.ieee.org/

2. Cisco Systems Training Materials
"Ethernet Technologies," Chapter 7, Internetworking Technology Overview, June 1999,
URL - http://www.cisco.com/

3. Fibre Channel (FC) Specifications
"Fibre Channel Physical Interfaces (FC-PI) Specification Revision 11"
URL - http://www.fibrechannel.com/

4. Agilent Application Notes (AN) and Data Sheets
- Product Data Sheet, "HFBR-5701L/5710L"
- Product Data Sheet, "HDMP-1687"
- AN 1166, "Minimizing Radiated Emissions of High Speed Data Communication Systems"
- White Paper, "HFBR-5701/5710/5730L(LP) SFP EMI Emissions Performance Enables High Port Count"
- AN 1242, "Reference Design for HFBR-5701L/5710L and HDMP-1687"
- AN 1237, "HFBR-0571 Evaluation Kit for Small Form-factor Pluggable (SFP) Transceivers"

URL - http://www.agilent.com/

5. "Stripline Components," Agilent Technologies Advanced Design System User Manual, Chapter 29.

6. Pozar, David M., Microwave Engineering, Addisson-Wesley Publishing Company, Inc., 1990, pp 417-426.

7. Small Form Factor Pluggable (SFP) Multi-Source Agreement
"Small Form-factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA)"
URL - http://www.agilent.com/

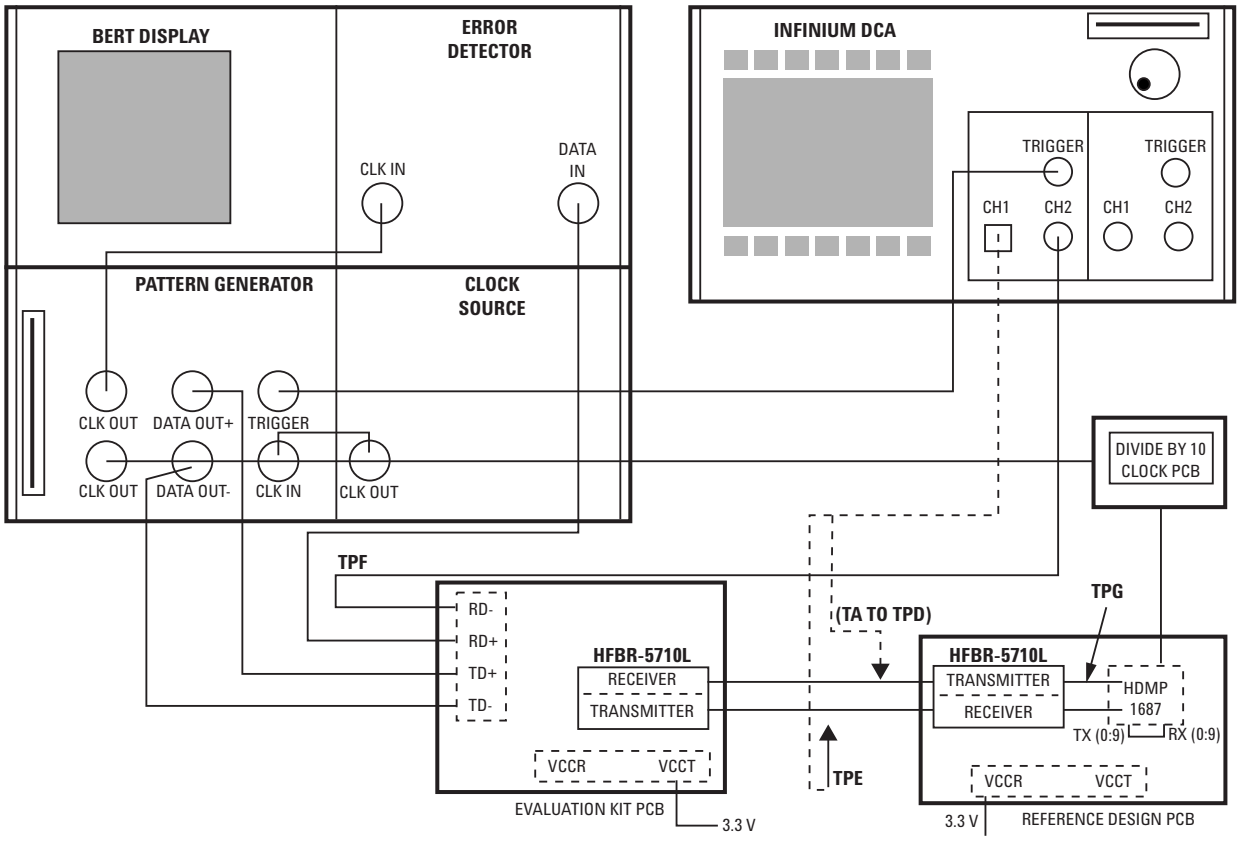
8. Optical Network Interface Design Symposium (ONIDS)
- "IBIS Modeling of High Speed Fiber Optic Components"
- "Optimizing Gigabit Idle Pattern for Better EMC Performance"

9. Network Equipment Building System (NEBS)
"NEBS GR-63 and GR-1089 Standards"
URL - http://www.telcordia.com/

10. National Committee for Information Technology Standardization (NCITS)

Appendix A.

Test Configuration



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